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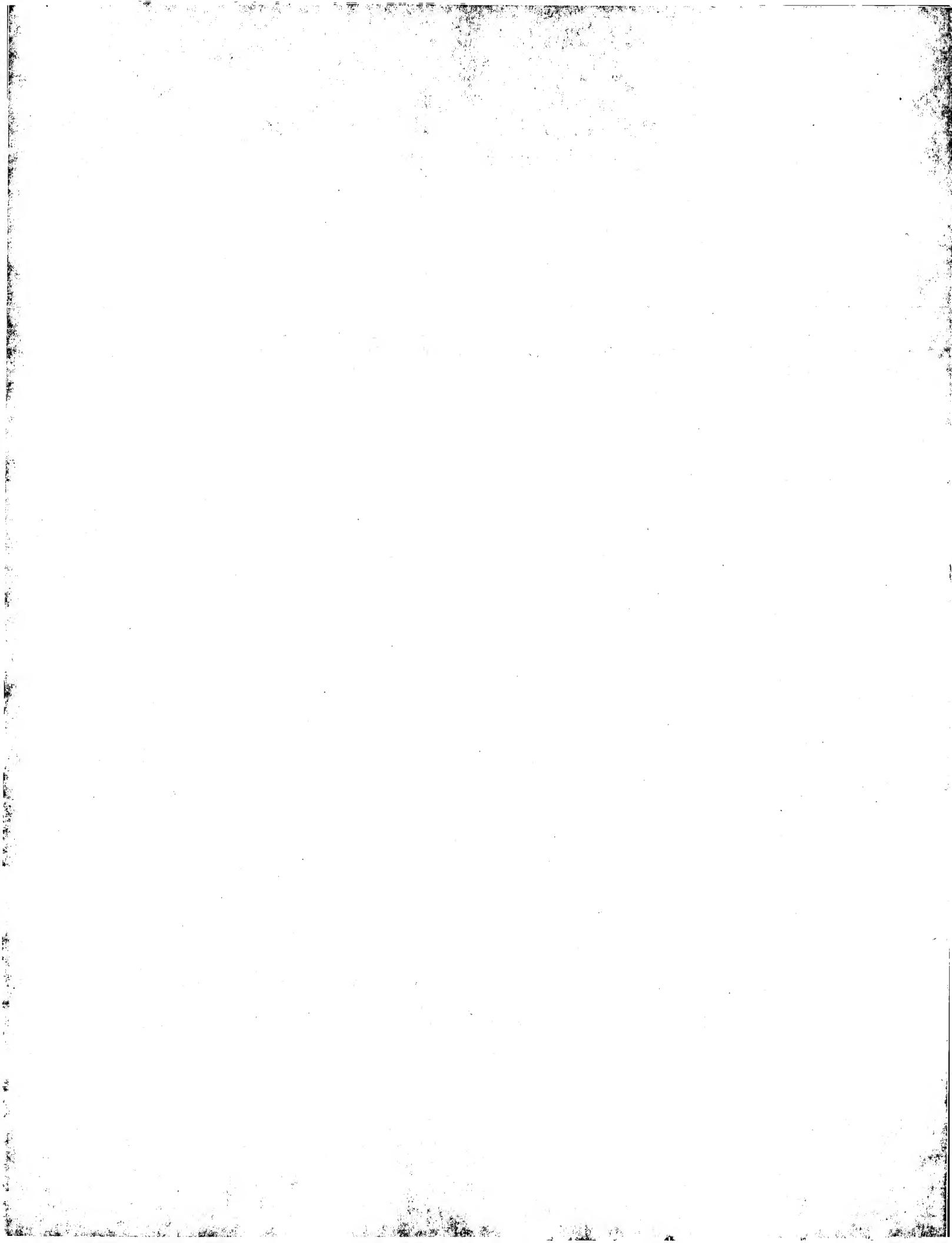
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(54) Switching current mode converter with reduced turn-on delay of power devices

(57) The turn-on delay of a current mode switching converter is reduced by modifying a normal error summing block so as to include

tor and outputting a pulse of a preestablished duration at the incoming of a rising front of the input signal;

- a window comparator to the input of which is fed the output voltage of the converter before being filtered by the low pass filter and to which a low threshold and high threshold reference voltages are applied, both of which are referred to the reference voltage of the converter;
- a differentiating circuit whose input is coupled to the so defined "under" output of the window compara-

- two amplifiers of the same gain K , both being enableable for outputting an amplified signal only when enabled; and
- two summing circuits, one adding the reference signal of the converter (V_{ref}), and the other the feedback signal of the output voltage filtered by the low pass filter to the respective signals amplified by said enabling amplifiers when enabled.

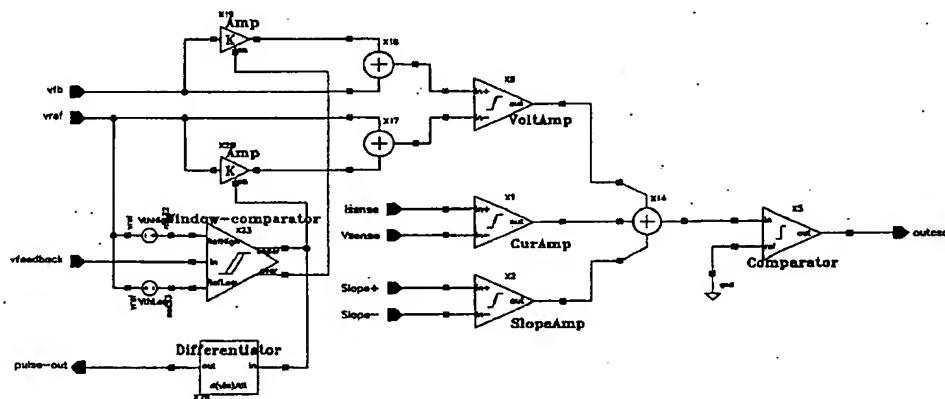


FIG. 3

Description**FIELD OF APPLICATION OF THE INVENTION**

[0001] The invention relates in general to switching DC-DC converters controlled in current mode and more in particular to techniques for speeding up the circuit response to sudden load variations, in particularly demanding applications.

BACKGROUND OF THE INVENTION

[0002] New generations of microprocessors are continuously and inexorably evolving. The need of processing an ever increasing amount of information in shorter and shorter times is leading the manufacturers of these devices to lower the voltage supply and increase the input current requisite.

[0003] Thence, modern microprocessors may require currents of many amperes (up to 50A at present), not in a continuos manner, but determined by the amount of operations to be processed at a certain instant. Therefore, the current absorbed may change from tens of mA to 10-12A in few nanoseconds and at present a common slew rate requirement is of about 5A/ns which is generally fulfilled thanks to an array of large capacitors, often placed in the socket mount of the microprocessor.

[0004] This solution does not relieve the power supply from quickly responding to the sudden need of current, the slew rate value which at present seems to be needed to maintain a stable level of the supply voltage of the array of capacitors is of about 30A/ μ s, a quite respectable figure which is not easily ensured.

[0005] The manufacturers of power supplies are adopting particular solution in trying to speed up the response of switching DC-DC converters used therein.

[0006] Current mode converters are by far the most widely used because of their good response characteristics. However, they require the use of a current sensing resistor of few Ohms connected in series to the inductor, leading to a power dissipation, which, by growing with the square of the output current of a DC-DC step-down converter, is becoming more and more unacceptable.

[0007] Thence, voltage mode solutions are gaining ground because they do not require such a dissipating sensing resistor. However, due to their slow response, they require special "tricks" to attain an acceptable speed of response.

[0008] A commonly adopted solution consists of placing two comparators about the reference voltage of the system. These comparators continuously check the real output voltage and act on the control loop at the instant in which a certain range is exceeded.

[0009] At present this is implemented in the commercial converters LTC1430 and LTC1553 manufactured by Linear Technology and in the series of devices 4900/01/02 of Microlinear, all functioning in a voltage

mode.

[0010] The response time of current mode converters is normally in the vicinity of a few clock cycles and therefore no need has ever been felt for increasing their response speed. Moreover, new current control techniques have made these types of converters an interesting solution even for high current applications (for instance, the technique of exploiting the RdsON of the external power MOS transistor for sensing the current).

[0011] In view of slew rate requisites as those cited above, it may become necessary to improve even the already fast response time of current mode converters to attain delay times that do not exceed a few hundred nanoseconds before the turn-on of the external MOS occurs.

[0012] Fig. 1 shows the scheme of a current mode Buck converter.

[0013] In the ensuing description reference will be made to this circuital topology even though the invention is similarly applicable to any other topology of switching converters, operating in a current mode.

[0014] The block indicated with the symbol Σ is the so called "error summing" block, whose internal diagram is shown in Fig. 2. This block Σ is responsible of stabilizing the system and of the precision of the output voltage. Indeed, this Σ block decides when to turn-off or turn-on the Hside and Lside power transistors of the switching converter.

[0015] The Σ block receives three distinct differential input signals: the error voltage of the comparison between the reference voltage and the output of the converter ($V_{ref}-V_{fb}$), the potential difference ($I_{sense}-V_{sense}$) on the sensing resistor connected in series to the output inductor L_f of the converter, the voltage signal (slope+ slope-) coming from the saw tooth oscillator which creates the ramp compensation. The error summing block Σ governs the turn-off of the Hside when the sum of the three contributing signals, with the indicated signs, reaches the zero value.

[0016] The low pass filter, LP-Filter, placed between the converter output and the error summing block Σ is needed for stabilizing the system, the pole introduced by the filter may range from a few kHz to tens of kHz, depending on the application.

[0017] The PWM-control-block manages all the control signals coming from the analog parts (zero-crossing comparators, under/over-voltage, etc.) and from the error summing block Σ itself and generates the signals for the MOS driver block which directly drives the external power MOS transistors.

[0018] In order to obtain systems operating at a constant frequency while the turn-off of the external MOS (Hside) is totally asynchronous and controlled by the Ersun signal, the turn-on cannot take place at any successive instant but rather, only in synchronism with the clock.

[0019] Unfortunately, this characteristic introduces a certain turn-on delay, whose maximum value is equal to

the clock period.

[0020] In other words, if the Ersum signal decided that a turn-on must take place again a few nanoseconds after a clock pulse, the turn-on may occur only at the next pulse and not immediately as decided by the Ersum signal.

[0021] Fig. 2 is the diagram of the error summing block Σ . The blocks X0, X1 and X2 usually are amplifiers of a very low gain (of a few units or of unity gain) and their contribution is summed in block X14 to produce a signal which is compared with the zero (gnd) by the output comparator X5, thus squaring the information in the form of a logic signal (outesc signal).

OBJECTIVE AND SUMMARY OF THE INVENTION

[0022] It has now been found a simple and efficient circuit to significantly reduce the turn-on delay of the order of the clock period as normally associated to a current mode switching converter, according to the known art.

[0023] This important result is attained, according to the present invention, by modifying the error summing block as it is normally realized according to known techniques, substantially without materially increasing its circuital complexity.

[0024] Essentially, additional blocks are placed upstream of the inputs of the error amplifier between the reference voltage and output voltage of the converter.

Basically these additional blocks comprise:

[0025]

- a window comparator to the input of which input is fed the output voltage of the converter before being filtered by the low pass filter and to which a low threshold and high threshold reference voltages are applied, both of which are referred to the reference voltage of the converter. The window comparator being fully differential and having a first and a second output, defined "under" and "over", respectively;
- a differentiating circuit whose input is coupled to the so defined "under" output of the window comparator and outputting a pulse of a preestablished duration at the incoming of a rising front of the input signal (under);
- two amplifiers of the same gain K, both being enableable for outputting an amplified signal only when they are enabled;
- two summing circuits, one adding the reference signal of the converter (V_{ref}), and the other the feedback signal of the output voltage filtered by the low pass filter to the respective signals amplified by said

enabling amplifiers when enabled.

[0026] The invention is specified in the annexed claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027]

10 Figure 1 shows the basic scheme of a current mode switching converter, as discussed above.

Figure 2 shows in more detail the Σ block of the converter of Fig. 1, as already described above.

15 Figure 3 is a diagram of the Σ block of Fig. 2, modified according to the present invention.

20 Figure 4 shows switching current mode converter similar to that of Fig. 1, with a modified Σ block according to the present invention.

25 Figures 5, 6, 7, 8, 9, and 10 show, for comparison purpose, the different behaviors of the known converter of Fig. 1 and of the converter made according to the present invention of Fig. 4, under different operating conditions.

DESCRIPTION OF AND EMBODIMENT OF THE INVENTION

30 [0028] By referring to the case of a switching DC-DC converter of the so-called Vac type controlled in current mode, whose typical circuit topology is reproduced in Figures 1 and 2, Figures 3 and 4 show the converter realized according to the present invention and highlight, by way of comparison, the additional elements that are introduced in accordance with the present invention. In particular, Fig. 4 shows the diagram of the error summing block Σ modified according to the invention. Upon comparing the diagram of Fig. 4 with the known diagram of Fig. 2, the following additional blocks are present:

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- 40 - a window comparator to which a $V_{feedback}$ voltage that is the unfiltered output voltage V_{out} of the converter is fed at its input, and to which two voltages, namely: V_{thHigh} and V_{thLow} are applied, both referred to the reference voltage V_{ref} , that is, to the control voltage reference of the converter and producing two output signals, namely: "under" and "over";
- 45 - a differentiator which at the incoming of a rising front of the signal "under" generates an output pulse whose duration is of about 100ns;
- 50 - two amplifiers of gain K, activated by the use of an enable signal; these amplifiers are normally off

(output at zero) and they output a signal $K \cdot V_{in}$ only when the respective enable signal is high;

- two summing circuits that sum the V_{fb} or V_{ref} signal to the respective $K \cdot V_{fb}$ or $K \cdot V_{ref}$ if the latter is not null.

LOAD VARIATION TOWARD HEAVIER VALUES DURING A TON PHASE

[0029] Fig. 5 illustrates the behavior of a known converter (Figures 1 and 2) during normal operating conditions. The figure depicts the V_{out} voltage of the converter, the V_{fb} voltage at the output of the feedback loop filter, the voltage V_{pwm} that is the voltage existing on the source of the Hside MOS transistor and the system's clock. The two dashed lines, just above and below the V_{out} , define the band of the window comparator used in the converter as modified according to the present invention. They are not pertinent to these diagrams that depict the behavior of the known converter of Fig. 1, but they are shown just for comparison.

[0030] Upon the varying of the load toward heavier values, the V_{out} drops abruptly of a value that depends on the R_{sense} and on the variation of the output current. Due to the low pass filter LP normally introduced for stabilizing the feedback loop, the V_{fb} voltage which is seen by the error summing block does not follow the actual variation of the output voltage V_{out} . Therefore the system does not sense the real variation and acts by correcting an error which is apparently of a lower magnitude. Hence, the duty cycle relative to the current clock pulse is not immediately expanded to the fullest extent, instead, the next clock pulse must be waited for the E_{sum} signal to eventually command the maximum correction, in presence of a further decreased V_{fb} .

[0031] Fig. 6 shows the same situation, but for the case of the converter of the invention depicted in Figures 3 and 4. The two thresholds: V_{th-up} (defined by the dedicated generator $V_{th-high}$) and $V_{th-down}$ (defined by the dedicated generator V_{th-low}) are set to an appropriate value that is chosen in consideration of the expected current variation and the value of R_{sense} , normally between $+/-50mV$ and $+/-100mV$. At the instant when the V_{out} voltage decreases abruptly because of the load variation, the $V_{th-down}$ threshold is exceeded and the window comparator X23 rises its output signal "under", which enables the X20 amplifier placed on the V_{ref} line. The correcting signal which was equal to:

$$V_{err} = V_{fb} - V_{ref}$$

and which at the moment was negative, is raised to the new value given by:

$$V_{eff} = V_{fb} - (1 + K) V_{ref}$$

which is clearly more negative.

[0032] Hence, this signal forces the error summing block Σ to correct a signal greater than the one that the LF-Ffilter would allow it to perceive, thus expanding the duty cycle of the current clock pulse, without waiting for the next pulse.

[0033] The gain factor K of the two amplifiers X20 and X19 may be freely chosen, the greater correction is obtained for a K that will "saturate" the duty cycle to its maximum value permitted by the MOS-driver.

[0034] Such value should be computed depending on the particular application though normal values at K should range between a few units and few tens of units.

[0035] In order to avoid undue interferences of the window comparator X23 during normal operation of the converter, specially when the ripple of the output voltage ($V_{out} + V_{fb}$) is near in the average to one of the two thresholds, it is better to make the window comparator X23 with a delay ranging between 100s and 200ns depending on the type of application. This will prevent that spikes, normally existing on the control voltage, may cause undue interventions and an irregular functioning of the switching controller PWM-control-Logic.

[0036] Fig. 6 shows the way the duty cycle has already been fully expanded to its maximum during the current clock pulse without waiting for a complete cycle.

[0037] To appreciate this advantage, the distance on the time axis between the instants of Figures 5 and 6 when the controlled V_{out} voltage is within the range in which the window comparator is disabled and thus the signal "under" low is highlighted. The indicated distance Δt is the measure of the advantage achieved in terms of faster response speed of the system.

[0038] The average value of Δt that may be achieved in current mode converters is of about half a clock cycle, meaning from $1\mu s$ to $5\mu s$, because the working frequency nowadays tends to be between 100kHz and 500kHz. Such an advantage may, in absolute terms, appear not very big, but the stringent speed requisites of power supplies for new generation μP impose to fully exploit it.

LOAD VARIATION TOWARD HEAVIER VALUES DURING A TOFF PHASE

[0039] If the load variation occurs at a Toff instant, a further block must be added to obtain the same effect described for the preceding case. Such a block is the differentiator X28 depicted in Fig. 3, which receives as an input the signal "under" output by the window comparator X23, and outputs a pulse whose duration may be of about 100ns at the incoming of a rising front of the signal "under".

[0040] The situation is substantially similar to that previously analyzed. The Figures 7 and 8 show, by way of comparison, the behavior of the classical converter of Figures 1 and 2 and of the converter of the invention of Figures 3 and 4, respectively. The substantial difference is that in this case the load varies (requiring more cur-

rent) while the MosHside is off, that is during the Toff phase. In the known converter (Fig. 7) there is a synchronous turn-on of the MosHside in synchronism with the next clock pulse available and, only if the loop filter has a sufficiently large time constant of a duration equal to the maximum duty cycle allowed by the system.

[0041] The waiting for the next clock pulse lets the output voltage V_{out} drop further to an undesirably low value. According to the invention, in order to improve this situation, the signal "under" used generated by the window comparator X23 is exploited, which upon the variation of the load turns on the K-gain amplifier X20 thus forcing the error summing block Σ to effect a larger than expected correction, as already explained above.

[0042] Such a signal "under" is fed to the input of the differentiator X28 which generates a pulse whose duration of about 100ns, approximately equal to that of the master clock. This pulse (pulse-out) is sent to the Added Clock input of the PWM-control-logic block, as shown in the diagram of Fig. 4, which simply adds it to the clock signal of the internal oscillator. The effect is shown in Fig. 8, where it may be observed how an asynchronous clock pulse is physically added to allow the system to turn on the MosHside at the very instant the load variation occurs and therefore to recover faster than a prior art system.

[0043] It is also observed that the error summing block Σ , at the time of sensing the downward exceeding of the V_{th-low} threshold, is internally forced in the position of maximum recovery by the signal "under" and therefore the duty cycle of the added pulse is already expanded to the fullest measure.

LOAD VARIATION TOWARDS LIGHTER VALUES

[0044] This condition of operation is relatively easier to control because the turn-off of the MosHside is not synchronous but asynchronous and controlled by the error summing block Σ and there is no need to output additional clock pulses.

[0045] Fig. 9 shows the usual trend of the output voltage V_{out} of a known current mode converter (Figures 1 and 2). Even in this case the voltage feedback to the error summing block by the loop filter tracks the real V_{out} , but with a certain delay, therefore, before an eventual complete turn-off, may appear, for a few clock cycles, some residual pulses because the voltage at the Ersum input of the PWM block is much lower than real. This provokes, even if in a less accentuated form than previously analyzed situations, a delay in relation to the theoretical recovery time of the system.

[0046] Fig. 10 shows the same situation, for the case of the converter of the invention of Figures 3 and 4.

[0047] When crossing the V_{th-up} threshold, the window comparator X23 rises the signal "over" that enables the amplifier X19 present on the V_{fb} line.

[0048] The correcting signal that was:

$$V_{err} = V_{fb} - V_{ref}$$

and therefore positive, is now raised to the new value given by:

$$V_{eff} = (1+K) V_{fb} - V_{ref}$$

which is evidently more positive and therefore is over corrected by the system by reducing the duty cycle more than it would otherwise do. Even in this case, the magnitude of the overforced correction may be chosen freely by changing the gain factor K of the amplifier X19; permissible values range between a few units to a few tens.

[0049] The achieved increment of the recovery speed, if compared to a classical current mode control system grows with the switching period and thereby with the decreasing of the working frequency of the converter.

20 Claims

1. A switching converter operating in a current mode comprising a pulse width modulation control logic (PWM-CONTROL-LOGIC) controlling a driving circuit (MOS DRIVER) of a half bridge power stage composed of a highside MOS device (MOS HSIDE) and by a low side MOS (MOSLSIDE) device connected in series between two supply nodes, a current sensing resistor (RSENSE) electrically in series to an output inductor (LP) of the converter a feedback comparator/amplifier block (Σ) a logic signal (OUTSEC) enabling the turn-on of at least one of said MOS devices in function of a positive result of the sum of at least three distinct differential signals input to said block (Σ), one of said three differential signals being an error signal between a feedback voltage (V_{fb}) filtered by a low pass loop filter (LP-FILTER), representative of the output voltage (V_{out}) of the converter, and a reference voltage (V_{ref}), further comprising means for reducing the recovery time of the converter's output voltage in case of abrupt load variations, characterized in that said means comprise

45 a window comparator (X23), to a first input of which is applied a signal ($V_{feedback}$) representative of the output voltage (V_{out}) of the comparator and to two other inputs of which are applied two threshold voltages (V_{thHigh} , V_{thLow}), both referred to said reference voltage (V_{ref}), and having a first output (under), and a second output (over) onto which a high logic signal is generated, respectively when the output voltage (V_{out}) of the converter exceeds either one (V_{thLow}) or the other (V_{thHigh}) of said two threshold voltages;

50 a differentiating circuit (X28) having an input

coupled to said first output (under) of said window comparator (X23) and an output coupled to a dedicated input for added clock pulses (ADDED-CLOCK) of said control logic (PWM-CONTROL-LOGIC);

5

a first amplifier (X19) enabled by a high logic signal present of said first output (over) of said window comparator (X23) and a first summing circuit (X16), functionally coupled to the input line of said filtered voltage (V_{fb}) to feedback a noninverting input of an error amplifier (X0) of said block (Σ);

10

a second amplifier (X20) enabled by a high logic signal present of said second output (under) of said window comparator (X23) and a second summing circuit (X17), functionally coupled to the input line of said reference voltage (V_{ref}) to an inverting input of said error amplifier (X0).

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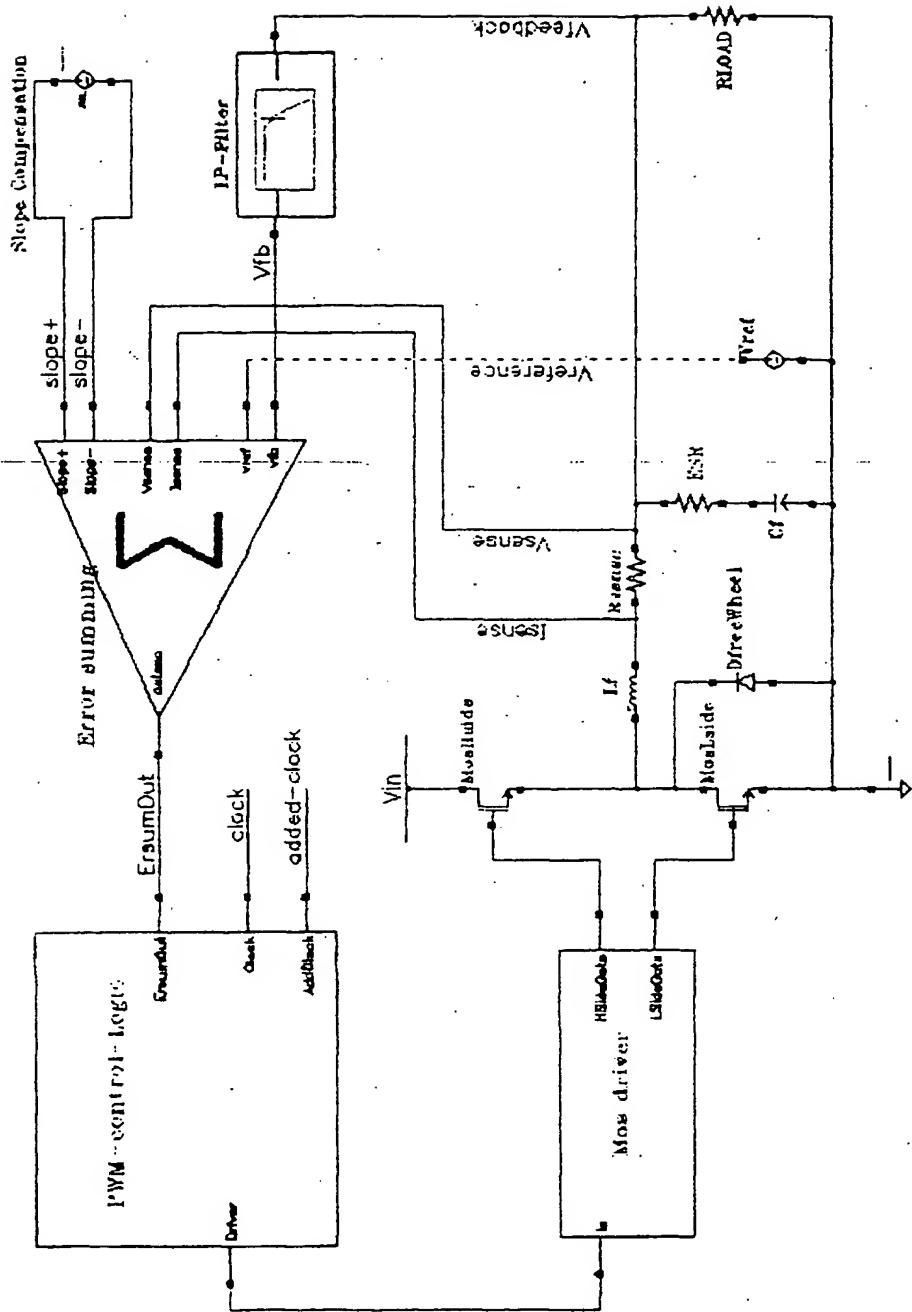
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FIG. 1



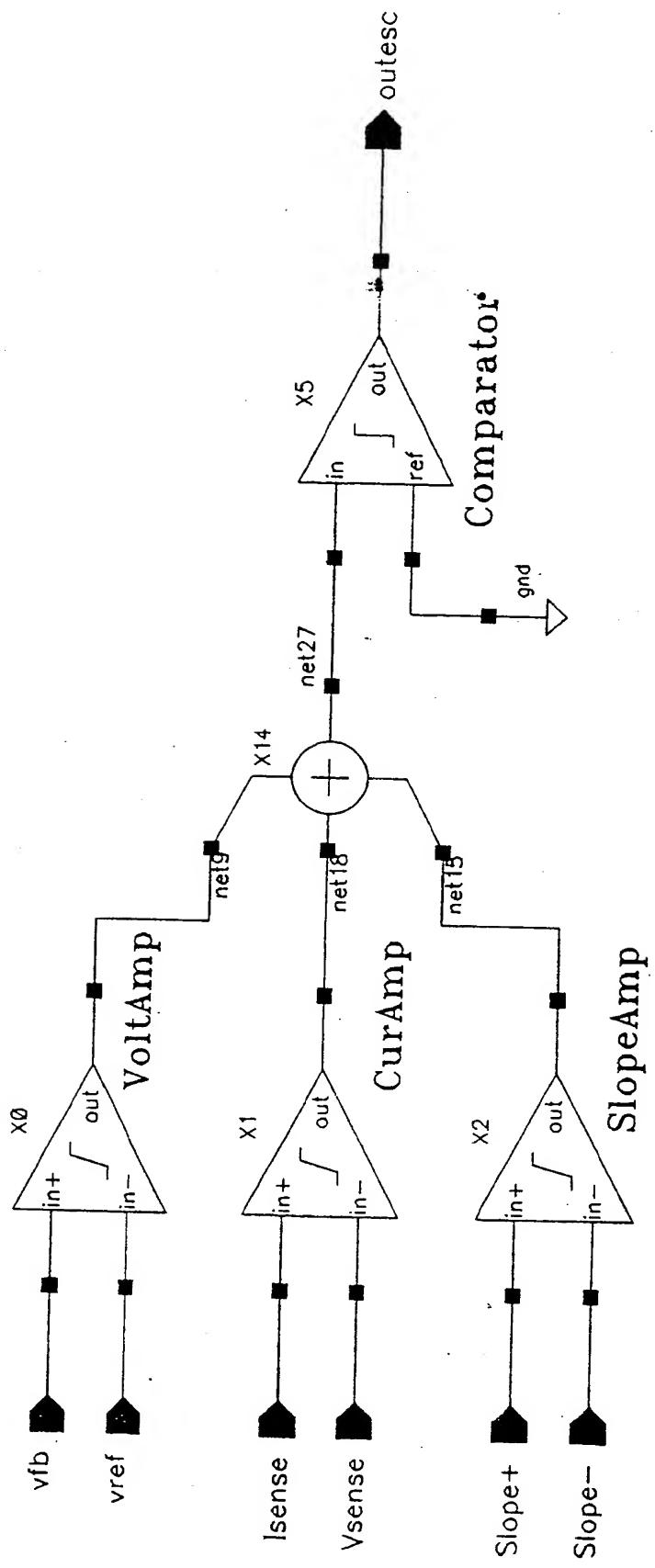


FIG. 2

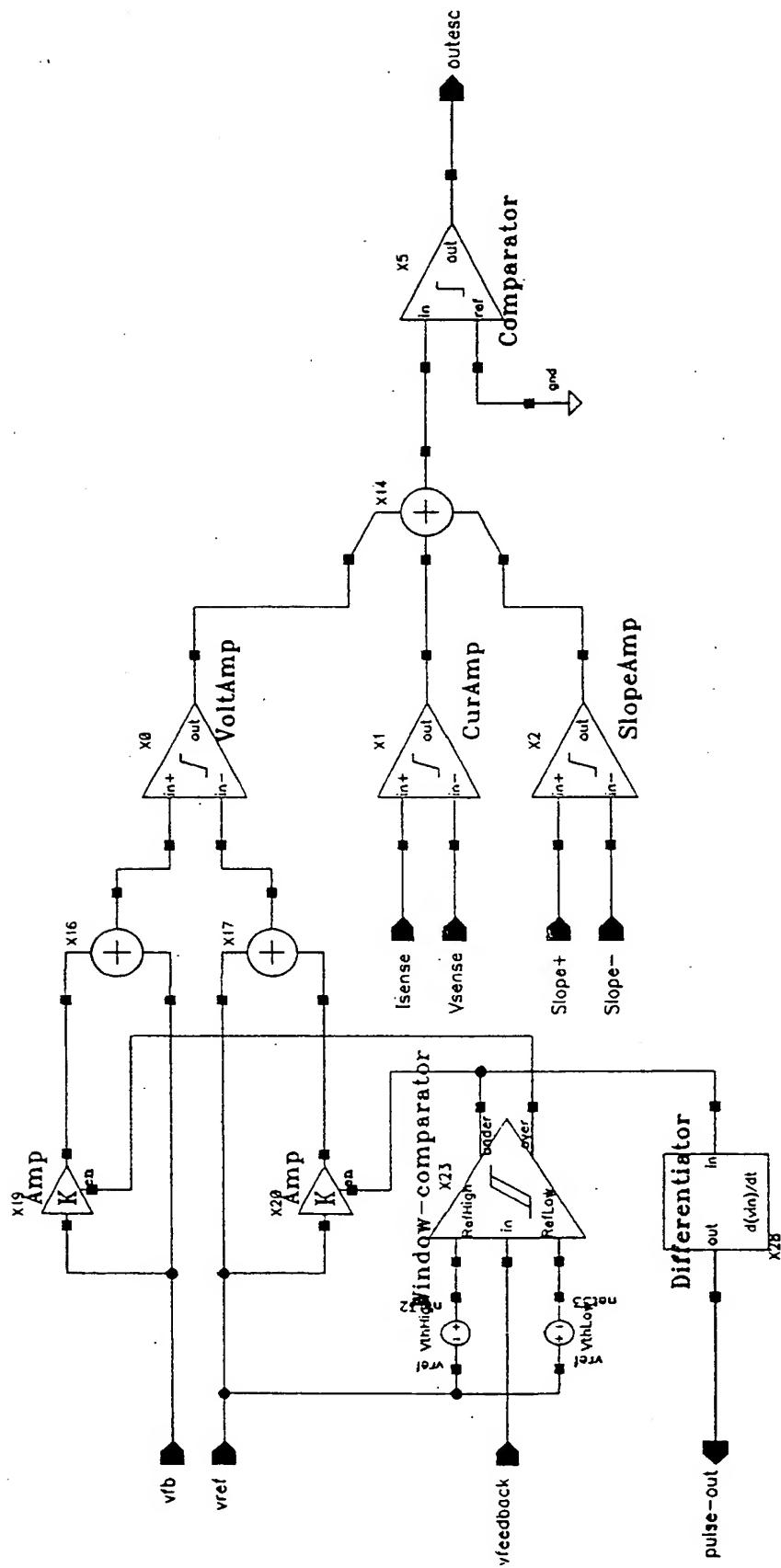


FIG. 3

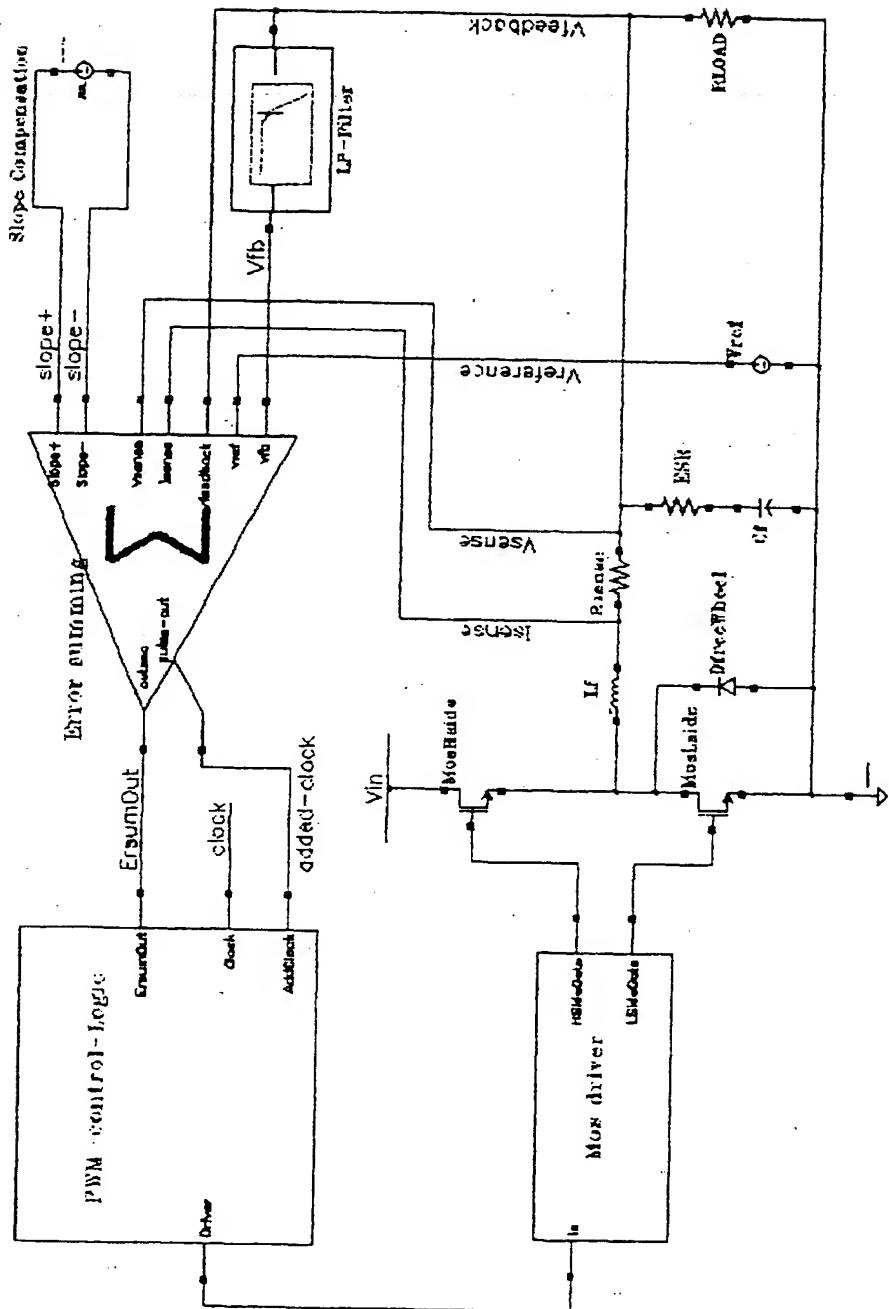
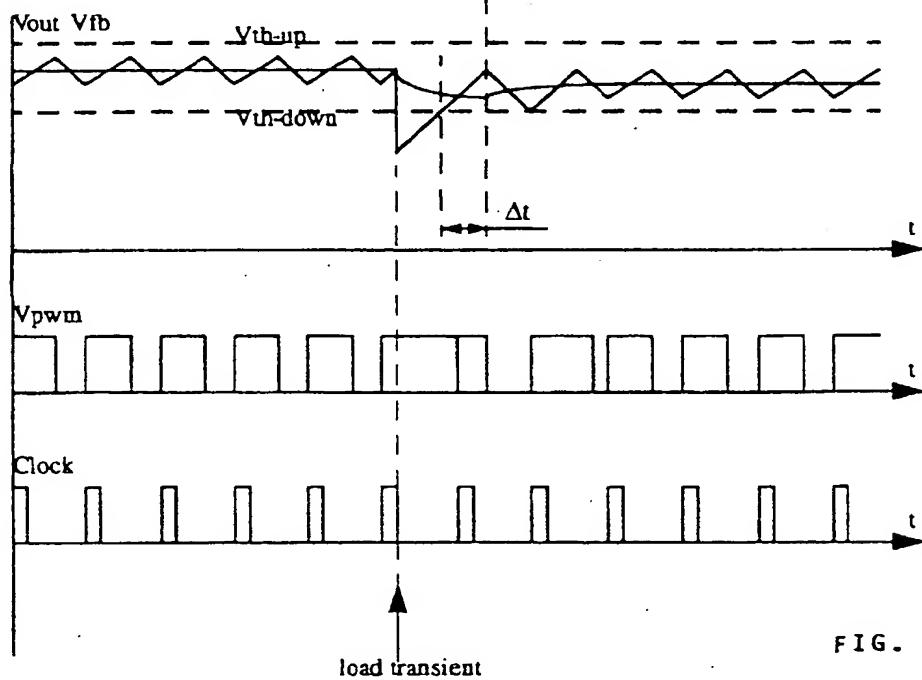
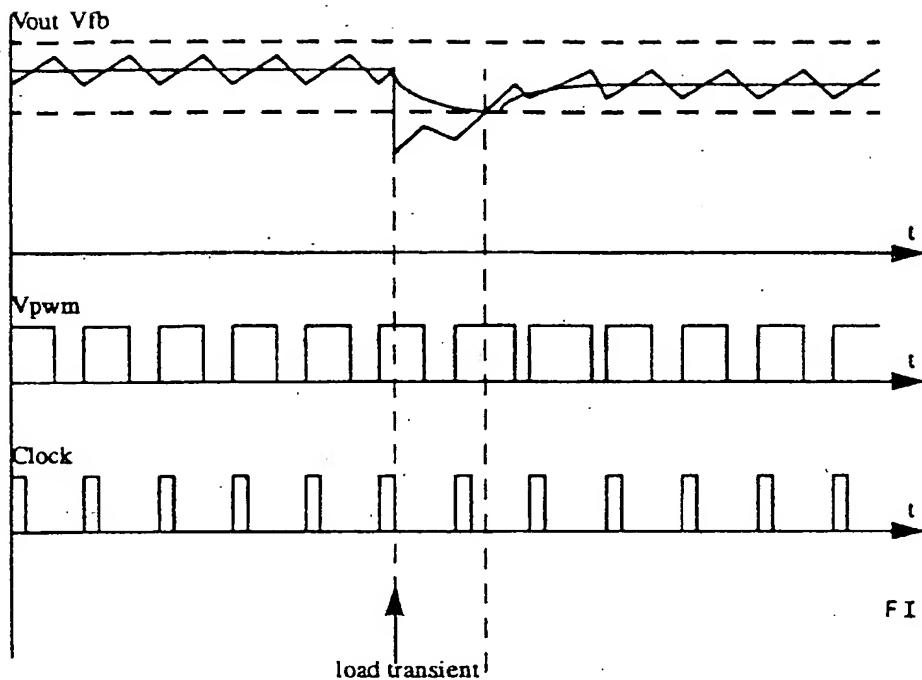
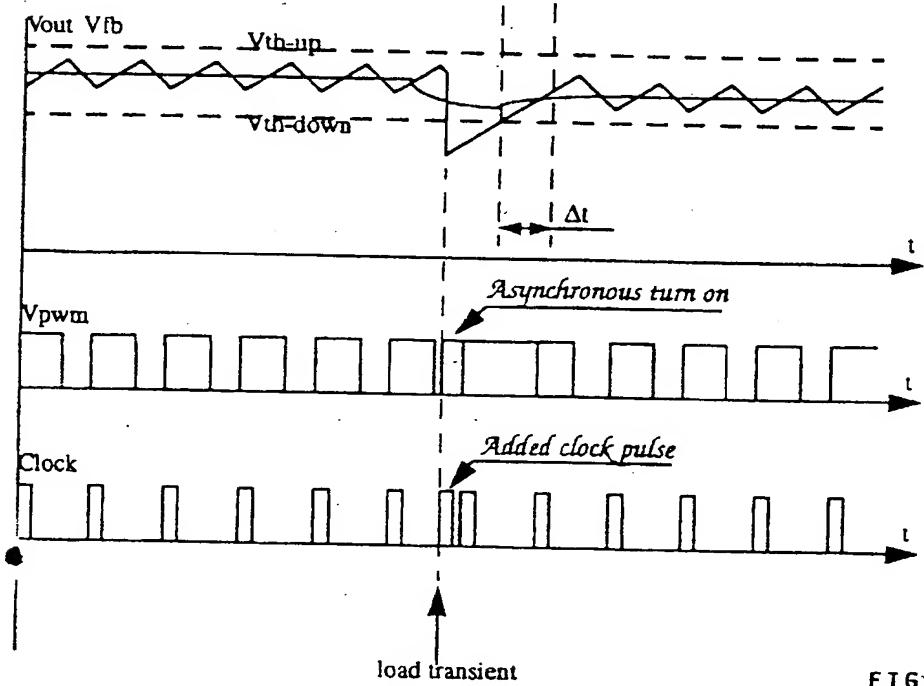
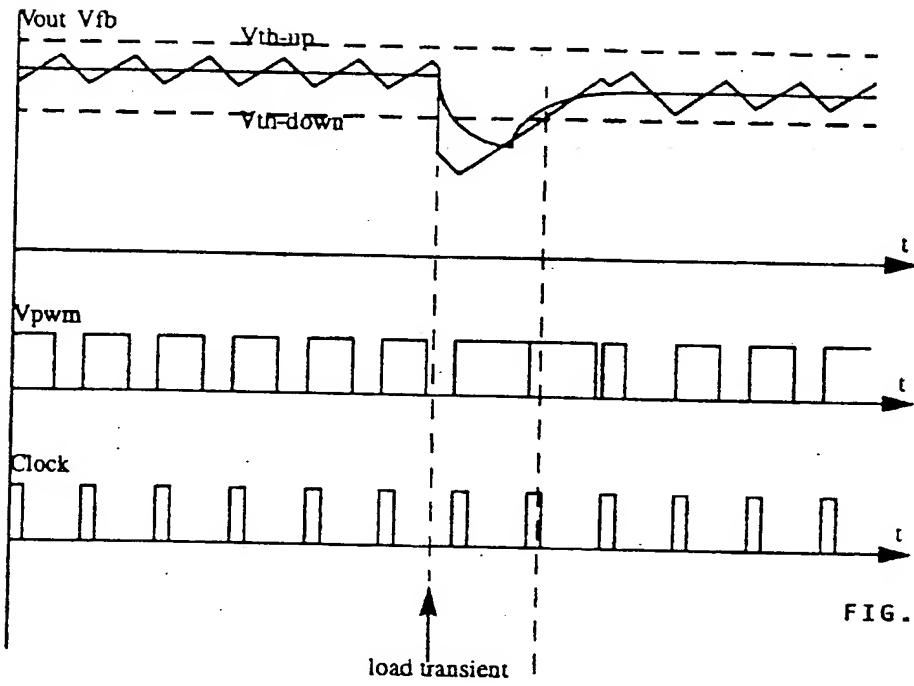
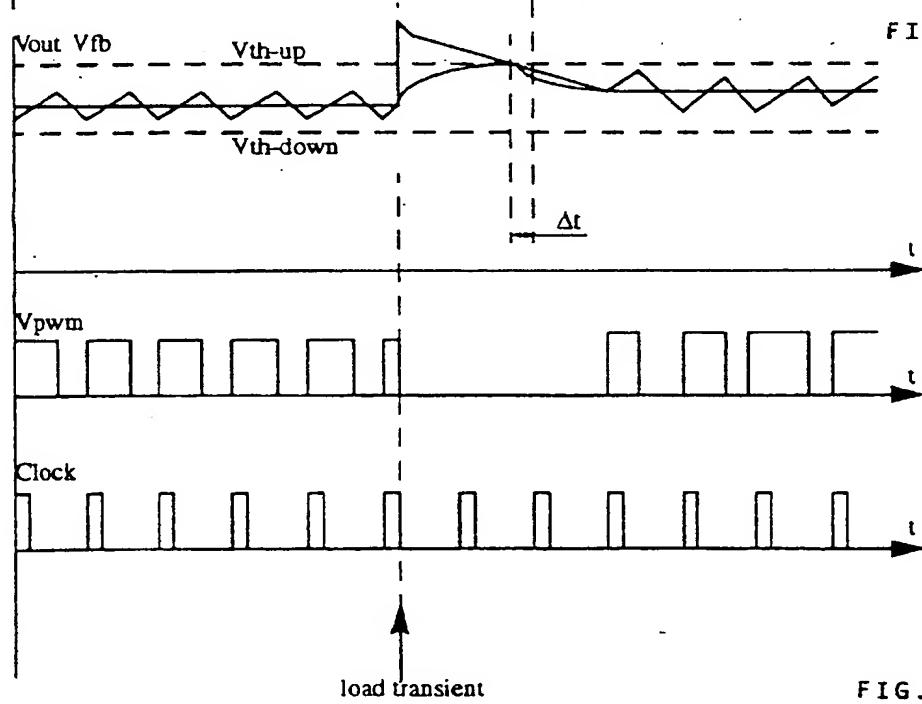
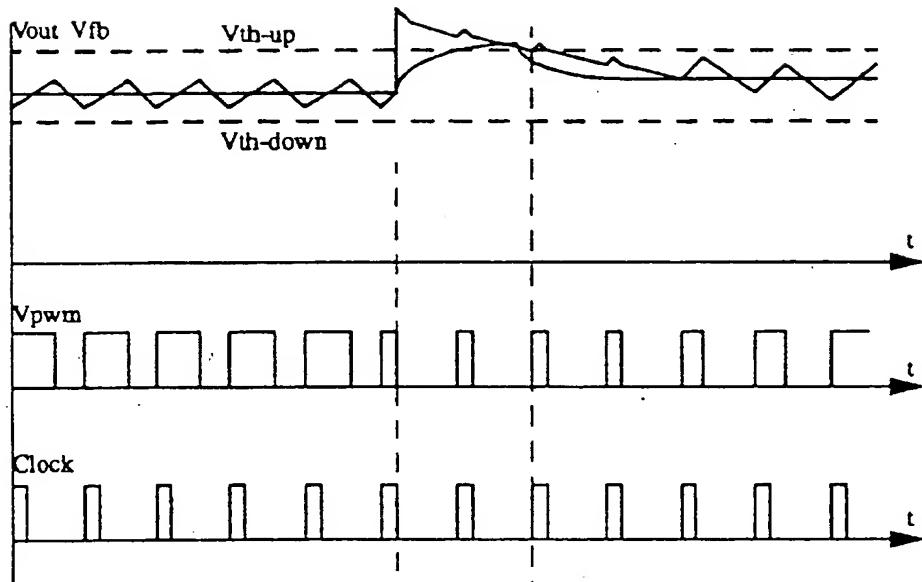


FIG. 4









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Application Number

EP 97 83 0459

DOCUMENTS CONSIDERED TO BE RELEVANT

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	GOODENOUGH F: "FAST LDOS AND SWITCHERS PROVIDE SUB-5-V POWER" ELECTRONIC DESIGN, vol. 43, no. 18, 5 September 1995, page 65/66, 68, 70, 72, 74 XP000535276 * the whole document *	1	H02M3/158 H02M3/337
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 371 (E-1113), 18 September 1991 & JP 03 145968 A (MITSUBISHI ELECTRIC CORP), 21 June 1991, * abstract *	1	
TECHNICAL FIELDS SEARCHED (Int.Cl.6)			
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The present search report has been drawn up for all claims			
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THE HAGUE	20 February 1998	Gentili, L	
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